IN THE CLAIMS

1-21. (Canceled)

22. (Previously presented) A computing system, said computing system comprising:

an input device and a computing device, said input device including a memory, a controller having a first CPU and an electronic pen input device operative to emit a first signal having a first characteristic and a second signal having a second characteristic, said computing device including a second CPU;

a detector for detecting said characteristics of the emitted signals; and

wherein said controller is interfaced with said detector so that said first CPU selectively interprets the emitted signals as one of information to be stored by said input device and information to be forwarded to said computing device and that routes (a) to said memory the information to be stored therein and (b) to the computing device the information to be forwarded thereto for processing by said second CPU.

23. (Previously presented) The computing system of claim 22 comprising a switch wherein the characteristic of said emitted signal is determined by operation of said switch.

24. (Previously presented) The computing system of claim 22, wherein said electronic pen input device comprises first and second tips that emit said first and second signals, respectively, and wherein which of said first and second signals is emitted depends on which one of said first and second tips is selected by a user.

25. (Canceled)

26. (Previously presented) The computing system of claim 25 wherein said memory comprises Flash RAM type memory.

27. (Previously presented) The computing system of claim 22, wherein said second CPU of said computing device responds to said information forwarded thereto based on detection of said second signal to control a display of said computing device.

28. (Previously presented) The computing system of claim 22, wherein said second CPU of said computing device responds to said information forwarded thereto based on detection of said second signal to control a function of said computing device.

29. (New) The computing system of claim 22, wherein said first CPU interprets said first signal as information to be stored in said memory and the second signal as information to be forwarded to said second CPU.